gate electrode as an ion implantation mask before the forming the spacer on the sidewalls of the gate electrode; and

forming a heavily doped impurity region by implanting high concentration impurity ions into the substrate using the gate electrode and the spacer as ion implantation mask before the forming the first preliminary trench.

9. The method of claim **1**, wherein a top surface of the SiGe epitaxial layer is as high as the top surface of the substrate.

10. The method of claim **1**, wherein a top surface of the SiGe epitaxial layer is higher than the top surface of the substrate.

11. A method of fabricating a semiconductor device comprising:

forming a gate electrode on a substrate;

forming a spacer on sidewalls of the gate electrode;

forming a first trench by etching a predetermined portion of the substrate exposed by the spacer and the gate electrode;

forming a sacrificial layer on a bottom surface of the first trench;

forming a second trench having a maximum width greater than that of the first trench by laterally etching the sidewalls of the first trench exposed by the sacrificial layer, wherein laterally etching the sidewalls of the first trench comprises anisotropically laterally etching the sidewalls of the first trench so that locations on opposing sidewalls of the second trench defining a maximum width thereof are closer to a top surface of the substrate than locations on the opposing sidewalls of the first trench defining a maximum width thereof;

etching the second trench to form a hexagonal profile epi-trench; and

forming a SiGe epitaxial layer in the hexagonal profile epi-trench.

12. A method of fabricating a semiconductor device comprising:

forming a sacrificial layer on a bottom surface of a preliminary trench;

etching sidewalls of preliminary trench in a substrate between immediately adjacent gate electrode structures to recess the sidewalls further beneath the gate electrode structures to provide recessed sidewalls, wherein etching the sidewalls of the preliminary trench comprises anisotropically laterally etching the sidewalls of the preliminary trench to provide upward-shifted profiles for the recessed sidewalls so that a curved profile of each of the recessed sidewalls is shifted upward toward a top surface of the substrate relative to respective profiles of the sidewalls of the preliminary trench, as a result of the anisotropically laterally etching of the sidewalls of the preliminary trench; and then

etching the recessed sidewalls and a bottom of the preliminary trench using crystallographic anisotropic etching to form a hexagonally shaped trench in the substrate; and

epitaxially growing a SiGe layer in the hexagonally shaped trench.

13. The method according to claim **12** wherein etching the recessed sidewalls comprises etching the recessed sidewalls to form outermost tips of the hexagonally shaped trench beneath the immediately adjacent gate electrode structures.

14. The method according to claim **13** wherein the outermost tips are aligned to sidewalls of the immediately adjacent gate electrode structures.

15. The method according to claim **13** wherein the outermost tips are 7 nm or less beneath a surface of the substrate.

16. The method according to claim **12** wherein forming a sacrificial layer comprises forming the sacrificial layer on the bottom surface of the preliminary trench and exposing at least a portion of the sidewall of the preliminary trench.

* * * * *